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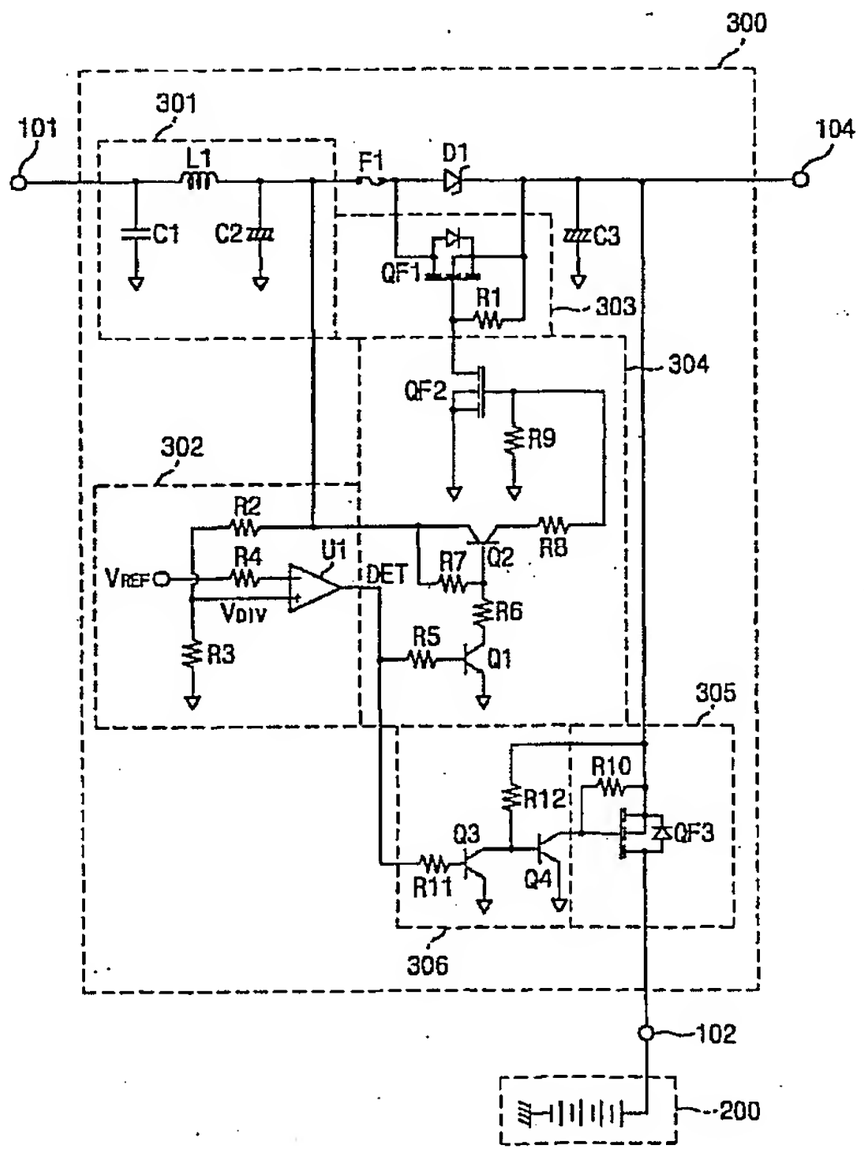
(54) Improved efficiency in power switching circuits

(57) A battery powered system comprises a switch circuit. In the switch circuit, a FET transistor is connected in parallel with a diode for preventing a current back flow from a battery to an external power source such as an AC adaptor. When the AC adaptor is supplying power, the FET transistor is turned on so that most of a current from the AC adaptor is delivered to a power supply line through the transistor instead of through the diode. Similarly, such switching circuits may be provided in a battery charging circuit. Because the current from the AC adaptor passes through FET transistors, power dissipation and loss by the switch and battery charging circuits can be reduced, and little heat is generated by the diodes.

Fig. 3



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Description

Background of the Invention

[0001] The present invention relates to electrical or electronic systems, and more particularly, to systems having two power sources, such as a battery and an AC adaptor.

[0002] Fig. 1 is a schematic diagram of an electronic system having a general power supply unit. In Fig. 1, power for the electronic system 10 is supplied by an external power source, that is, an AC adaptor 12, or a battery 13 (which may be a backup battery). The AC adaptor 12 is a device that converts an AC voltage from an external power source into a DC voltage. The AC adaptor 12 is connectable via a power supply line 11 to the electronic system 10. The electronic system 10 comprises a DC/DC converter 14 connected to power supply line 11. The DC/DC converter 14 is a device that controls the voltage that is supplied to the system load 15.

[0003] More specifically, the DC/DC converter 14 is coupled by supply line 11 to both the AC adaptor 12 and the battery 13. The DC/DC converter 14 reduces the voltage (for example, 19V), of the external power source (AC adaptor 12), or the voltage (for example, 7.4V to 15V) of the battery 12, to a constant voltage level (for example, 5V or 3.3V) that is appropriate for the operation of the system load 15.

[0004] The system load 15 represents the component in the electronic system 10 that consumes power and is driven by the constant DC voltage which is supplied by the DC/DC converter 14. If the electronic system 10 is a notebook computer, then a CPU, a memory, a display or individual peripherals are included as part of the system load 15.

[0005] In an electronic system that receives, in parallel, the output voltages of the AC adaptor 12 and the battery 13, means are required to prevent the flow of a reverse current caused by a voltage difference between the output voltages of the two power sources. In particular, when the battery 13 is supplying power, means must be provided to prevent a current back flow from the battery 13 to the AC adaptor 12 via the power supply line 11. Such a reverse current would result in wasteful power consumption by the AC adaptor 12, and wasteful discharge of the battery 13, which has a finite capacity.

[0006] Generally, a diode is inserted into the power supply line 11 of the external power source (AC adaptor 12) to allow only one direction of current flow: from the AC adaptor 12 to the DC/DC converter 14. In this way, when the output voltage of the battery 13 is higher than that of the AC adaptor 12, a back flow of current into the AC adaptor 12 is prevented or at least reduced.

[0007] However, any diode will introduce a voltage drop across its terminals when forward biased. It will dissipate power according to the forward voltage drop and the current it is carrying.

[0008] The diode may be a Schottky diode or a fast recovery diode. Since the voltage drop in the forward direction for the Schottky diode is relatively low (0.4V to 0.5V), this diode can effectively reduce the power that is wasted. Even so, the Schottky diode will dissipate power and will heat up. At high temperatures, reverse current through the Schottky diode is increased, so that the prevention of reverse current flow is not effective. On the other hand, although the voltage drop of a fast recovery diode in the forward direction is large (0.8V to 1.0V) (and so power dissipation and heating will be greater), current back flow is substantially lower when compared with that for a Schottky diode, even at high temperatures. Thus, a fast recovery diode can be used. A fast recovery diode, however, may become overheated because the voltage drop in the forward direction causes consideration power consumption. For example, with a 40W AC adaptor 12 supplying a current of 3A, the power consumed by a fast recovery diode is 2.4W to 3.0W (3A x 0.8V to 1.0V), such that a heat sink (for example, a cooling pan or a metal plate) is required.

[0009] As described above, a fast recovery diode or a Schottky diode is employed to prevent a reverse current flow from the battery 13 to the AC adaptor 12. However, since heat is generated by each of these diodes, means to discharge this heat is required, entailing expense in manufacture, wasteful power consumption, and unwanted heating of the equipment.

Summary of the Invention

[0010] It is therefore an object of the present invention to provide a system which may be powered by a battery, and an external power source such as an AC adaptor. Such a system preferably has an improved power efficiency and a reduced power dissipation and loss. Preferably, the heat generated by diodes, themselves used for preventing or reducing a current back flow, is reduced.

[0011] According to an aspect of the present invention, there is provided a switch circuit for use with a battery and an external power supply. Preferably, the switch circuit comprises a power supply line; a diode coupled in series between the power supply line and a terminal for coupling to an external power supply; and a switch coupled in parallel with the diode. The switch has a voltage drop when conductive, lower than that of the diode. A voltage (or current) detector for detecting whether a voltage (or a current) supplied by an external power supply is higher than a predetermined level, and generating a detection signal as a result, is included. A switch controller is also included, receiving the detection

signal, for controlling the ON/OFF condition of the switch so as to bring the switch into an ON condition when the voltage supplied by the external power supply is higher than the predetermined level.

[0012] The switch circuit may further comprise a second switch for coupling the power supply line to a battery; and a second switch controller receiving the detection signal, for controlling the ON/OFF condition of the second switch so as to bring the second switch into an OFF condition when the voltage or current supplied by the external power supply is higher than the respective predetermined level.

[0013] According to an aspect of the invention, a system comprises a switch circuit as described; a system load; a battery; and an external power supply, wherein power may be supplied to the system load over the power supply line, from either the battery or the external power supply, according to a status of the switching circuit.

[0014] The system may further comprise a voltage converter coupled to the system load, for controlling a voltage supplied to the system load.

[0015] The system may be a computer system.

[0016] The system load may comprise a memory, a direct memory access controller and a peripheral.

[0017] The system may be a portable system.

[0018] According to an aspect of the invention, a battery charging circuit comprises a first terminal for coupling to an external power supply; a second terminal for coupling to a battery; and a switch circuit as described, wherein the diode and the power supply line are coupled in series between the first terminal and the second terminal.

[0019] According to an aspect of the invention, a method of operating a switch circuit for providing power from a power supply to a power supply line is provided. The switch circuit comprises a diode coupled in series between the power supply line and a terminal for coupling to the power supply; and a switch coupled in parallel with the diode, the switch having a voltage drop when conductive, lower than that of the diode. The method comprises the steps of detecting whether a voltage, or a current, supplied by the power supply is higher than a predetermined level; and controlling the ON/OFF condition of the switch so as to bring the switch into an ON condition when the voltage, or current, respectively, supplied by the external power supply is higher than the predetermined level.

Brief Description of the Drawings

[0020] The objects, characteristics and advantages of the present invention will become apparent in the following description of certain embodiments, given by way of examples only, with reference to the accompanying drawings, in which:

Fig. 1 shows a schematic diagram of an electronic system having a general power supply unit;

Fig. 2 is a block diagram illustrating the configuration of a computer system according to an embodiment of the present invention;

Fig. 3 shows an embodiment of a switch circuit illustrated in Fig. 2;

Fig. 4 shows an embodiment of a first switch controller illustrated in Fig. 3;

Fig. 5 shows an embodiment of a battery charging circuit illustrated in Fig. 2; and

Fig. 6 shows an embodiment of a switch controller illustrated in Fig 5.

Detailed Description of the Drawings

[0021] Fig. 2 is a block diagram illustrating a computer system according to an embodiment of the present invention. In Fig. 2, an AC adaptor 100, connectable to the computer system, is connected to a commercially available external power source (not shown), such as an AC mains supply. The adaptor 100 rectifies and smoothes an AC voltage from the external power source to supply a DC voltage to the computer system.

[0022] The battery 200 can be recharged, optionally rapidly charged, by a battery charging circuit 400. Both battery 200 and battery charging circuit 400 can be built into the computer system. If the AC adaptor 100 is not connected to the computer system, or is not operating, and the battery 200 is connected, a DC voltage is supplied through a switch circuit 300 from the battery 200 to the respective components of the computer system in order to activate the computer system. A nickel-hydrogen battery is used as the battery 200, for example.

[0023] As shown in Fig. 2, a microcomputer power supply unit 500, a microcomputer 501, a DC/AC inverter 510, a liquid crystal display (LCD) 511, a DC/DC converter 520, and a system load 521 are further provided in the computer system. Although not shown in the figure, the system load 521 may typically comprise a ROM (read only memory) for

storing a control program inherent to the computer system, a RAM (random access memory), a direct memory access controller (DMAC) for performing the direct memory access control, a programmable interrupt controller (PIC) settable by a program, an expansion RAM with a large capacity and connectable to a special card slot, and a backup RAM for storing backup data, etc to implement a resume function.

[0024] The switch circuit 300 delivers a DC voltage from the AC adaptor 100, or a DC voltage from the battery 200, to the respective components of the computer system. In particular, when the AC adaptor 100 is connected to the computer system, the switch circuit 300 supplies the DC voltage from the AC adaptor 100 to the respective components of the computer system, while it stops supplying the DC voltage from the battery 200. If the AC adaptor 100 is detached from the computer system, the switch circuit 300 supplies the DC voltage from the battery 200 to the microcomputer power supply unit 500, the DC/AC inverter 510, and the DC/DC converter 520.

Switch Circuit

[0025] Fig. 3 is an embodiment of the switch circuit 300 according to an aspect of the present invention. The switch circuit 300 has a first input terminal 101 for connection with the AC adaptor 100; a second input terminal 102 for connection with the battery 200; and an output terminal 104 (or a power supply line) connected to, for example, the DC/DC converter 520. The switch circuit 300 connects the power supply line 104 to the AC adaptor when the AC adaptor 100 is connected to the input terminal 101. When the AC adaptor 100 is detached from the input terminal 101, the switch circuit 300 connects the power supply line 104 to the battery 200.

[0026] A filter 301 is coupled to the input terminal 101 and percolating a noise of the DC voltage. A fuse F1 is coupled between the filter 301 and a diode D1, itself coupled between the fuse F1 and the power supply line 104. Diode D1 prevents or reduces current back flow from the battery 200 to the AC adaptor 100. The diode D1 is preferably composed of a Schottky diode or a fast recovery diode.

[0027] A voltage detector 302, first and second switches 303 and 305 and first and second switch controllers 304 and 306 are further provided in the switch circuit 300.

[0028] The voltage detector 302 in this embodiment comprises three resistors R2, R3 and R4 and an operational amplifier or "op-amp" U1 (acting as a comparator). One end of the resistor R2 is connected via the filter 301 to the input terminal 101, and the other end of the resistor R2 is connected to the non-inverting input of the op amp U1, and through the resistor R3 to ground. With this arrangement, the resistors R2 and R3 act as a voltage divider so as to supply a divided voltage V_{DIV} to the non-inverting input of the op amp U1. Further, the inverting input of the op amp U1 receives a reference voltage V_{REF} through the resistor R4. The reference voltage V_{REF} is a voltage used as a power supply of the microcomputer 501.

[0029] When the inverting input voltage V_{REF} of the op amp U1 is higher than the non-inverting input voltage V_{DIV} thereof, (such as when the AC adaptor is not connected and the battery 200 is supplying power), the op amp U1 outputs a signal DET of a logical low level as a detection result. When the inverting input voltage V_{REF} of the op amp U1 is lower than the non-inverting input voltage V_{DIV} thereof, the op amp U1 outputs the signal DET of a logic high level. Such a high level signal indicates that the AC adaptor 100 is supplying power.

[0030] The switch 303 in this embodiment is provided by a P-channel power MOSFET transistor QF1 having a drop voltage of about 0.014V, and a resistor R1. The drain of the FET switch QF1 is connected to the input terminal 101 via the fuse F1 and the filter 301. The gate of FET switch QF1 is coupled to the corresponding switch controller 304, and the source of the FET switch QF1 is coupled to the power supply line 104. The resistor R1 is coupled between the source and the gate of the FET switch QF1. The drain of the transistor QF1 is coupled to an anode of the diode D1 and the source of the transistor QF1 is connected to a cathode of the diode D1. The source and body of transistor QF1 are connected together. Fig. 3 illustrates the drain/source diode, inherent in FET transistors, in parallel with the channel.

[0031] When the MOSFET transistor QF1 is not biased (is turned off), a current from the AC adaptor 100 is transferred via the diode D1, having a forward voltage drop of about 0.5V, to the power supply line 104, that is, the computer system. If the transistor QF1 is biased (is turned on), almost all the current from the AC adaptor 100 flows to the power supply line 104 via the FET transistor QF1 instead of via the diode D1.

[0032] Referring to Fig. 3, the first switch controller 304 receives the output signal DET from the voltage detector 302, and controls the ON/OFF condition of the FET transistor QF1 in the switch 303 so as to bring the transistor QF1 into an ON condition when the voltage of the AC adaptor 100 is higher than the reference voltage V_{REF} (ie when DET is high). The switch controller 304 controls the activation and inactivation of the switch circuit 303 in response to the signal DET from the voltage detector 302. The controller 304 comprises of five resistors R5 to R9, an N-channel FET transistor QF2, an NPN transistor Q1 and a PNP transistor Q2.

[0033] One end of resistor R5 is connected to the output DET of the voltage detector 302, and the other end of resistor R5 is coupled to a base of the transistor Q1 whose emitter is grounded. The collector of the transistor Q1 is connected via resistor R6 to the base of transistor Q2, whose emitter is connected to the input terminal 101 through the filter 301. Resistor R7 is connected between the emitter and the gate of the transistor Q2. The FET transistor QF2

has its gate connected via resistor R8 to the collector of transistor Q2, and has its drain coupled to the gate of the FET transistor QF1. Its source and body terminals are grounded. Further, the gate of the transistor QF2 is connected to ground via resistor R9.

[0034] When the signal DET from the voltage detector 302 is at a logic low level, that is, the inverting input voltage V_{REF} of the op amp U1 is higher than the non-inverting input voltage V_{DIV}, (indicating that AC adaptor 100 is not providing power), the transistors Q1 and Q2 are turned off. The transistor QF2 is also turned off, so that no bias voltage is applied between the gate and the source of the FET transistor QF1. Accordingly, FET transistor QF1 is turned off.

[0035] On the other hand, when the signal DET is at a logic high level, that is, the inverting input voltage V_{REF} of the op amp U1 is lower than the non-inverting input voltage V_{DIV}, (indicating that AC adaptor 100 is providing power), the transistors Q1 and Q2 are turned on. The FET transistor QF2 is turned on, and a bias voltage is applied between the gate and the source of the FET transistor QF1, caused by a current flowing from line 104 through resistor R1 to ground, via transistor QF2 and resistor R9. The FET transistor QF1 is turned on.

[0036] Second switch 305 is connected between the power supply line 104 and the input terminal 102. Switch 305 is comprised of a resistor R10 and a P-channel power FET transistor QF3. The source of the FET transistor QF3 is connected to the power supply line 104 and the drain is connected to the terminal 102. The gate of the FET transistor QF3 is connected to the second switch controller 306. The gate and the source of the transistor QF3 are also connected together through resistor R10. The source and body of transistor QF3 are connected together. Fig. 3 illustrates the drain/source diode, inherent in FET transistors, in parallel with the channel.

[0037] The second switch controller 306 receives the output signal DET from the voltage detector 302 and controls the ON/OFF condition of the FET transistor QF3 in the second switch 305. FET transistor QF3 is turned OFF by a high level signal DET when the voltage V_{DIV} representing the voltage of the AC adaptor 100 is higher than the reference voltage V_{REF}. The controller 306 is comprised of two resistors R11 and R12 and two NPN transistors Q3 and Q4. The base of the transistor Q3 is connected to the DET output of the voltage detector 302 through the resistor R11. The emitter of transistor Q3 is grounded, and the collector is connected to the base of transistor Q4. The emitter of transistor Q4 is grounded and the collector is coupled to the gate of the FET transistor QF3. Further, the collector of the transistor Q3 and the base of the transistor Q4 are coupled via resistor R12 to the source of the FET transistor QF3 and the power supply line 104.

[0038] When the output signal DET from the voltage detector 302 is at a logic high level (indicating that the AC adaptor 100 is supplying power), a bias voltage is applied between the base and the emitter of the transistor Q3 and the base of the transistor Q4 is grounded by conduction through transistor Q3. The transistor Q4 is turned off. No bias voltage is applied between the gate and the source of FET transistor QF3, and the FET transistor QF3 is turned off. The AC adaptor 100 is supplying power through diode D1 and/or FET transistor QF1.

[0039] On the other hand, when the signal DET is at a logic low level (indicating that the AC adaptor is not supplying power), the transistor Q3 is turned off. Since the transistor Q4 is biased by battery 200 through the diode of FET transistor QF3 and resistor R12, it is turned on. A bias voltage is applied between the gate and the source of FET transistor QF3, and it is turned on. A current flows via the turned-on FET transistor QF3 from the battery 200 to the power supply line 104.

[0040] The operation of a switch circuit 300 according to an embodiment of the present invention will be more fully described.

[0041] When the AC adaptor 100 is detached from the terminal 101, (ie, it is not supplying power), the non-inverting input voltage V_{DIV} of the op amp U1 in the voltage detector 302 is maintained lower than the inverting input voltage V_{REF} of the op amp U1, so that the output signal DET of the op amp U1 becomes logically low. This forces the second switch controller 306 to activate the second switch 305. In particular, since the signal DET is at a logic low level, the transistor Q3 is turned off and the transistor Q4 is turned on as described above. A bias voltage is applied between the gate and the source, and the FET transistor QF3 is turned on. Accordingly, the power supply line 104 is connected to the battery 200.

[0042] At the same time, the first switch controller 304 forces the first switch 303 to be turned off. In particular, when the inverting input voltage V_{REF} of the op amp U1 is higher than the non-inverting input voltage V_{DIV}, the signal DET is low, and the transistors Q1, Q2 and QF2 are turned off. No bias voltage is applied between the gate and the source of FET transistor QF1, which is then turned off. A current flow from the battery 200 to the AC adaptor 100 is prevented, or at least reduced, by the diode D1, so that a current back flow from the battery 200 to the AC adaptor 100 will not occur.

[0043] On the other hand, when the AC adaptor 100 is connected and supplying power to the terminal 101, a current from the AC adaptor 100 is initially transferred via the diode D1 to the power supply line 104. The non-inverting input voltage V_{DIV} of the op amp U1 in the voltage detector 302 becomes higher than the inverting input voltage V_{REF} of the op amp U1, and the op amp U1 outputs the signal DET of a logic high level. This makes the transistor Q3 of the second switch controller 306 turned on and the transistor Q4 turned off. No bias voltage is applied between the gate and the source of the FET transistor QF3, which is turned off. Accordingly, the battery 200 stops supplying a current for the power supply line 104.

[0044] Upon receipt of the signal DET of a logic high level from the voltage detector 302, the transistors Q1, Q2 and QF2 of the first switch controller 304 are turned on as described above. A bias voltage is applied between the gate and the source of FET transistor QF1, which is then turned on. This makes almost all the current from the AC adaptor 100 flow to the power supply line 104 through the first switch 303 instead of through the diode D1. This is because the diode D1 has a forward drop voltage of about 0.5V and the FET transistor QF1 has a drop voltage of only about 0.014V.

[0045] According to the switch circuit 300 of this embodiment, when a current from the AC adaptor 100 is first supplied, it flows through the diode D1. Then, the current flows through the FET transistor QF1 of the switch 303 instead of through the diode D1. Therefore, power dissipation and loss by the diode D1 can be reduced, so that practically no heat is generated by the diode D1 while the AC adaptor 100 is supplying power. This will be further described below.

[0046] Referring to Fig. 4, another embodiment of a first switch controller is illustrated. First switch controller 304' comprises four resistors R13 to R16, one op amp U2 and an N-channel MOSFET transistor QF4 connected as illustrated in Fig. 4. When an inverting input voltage V_{REF} (such as a voltage used as power of the microcomputer 501) of the op amp U2 is higher than a non-inverting input voltage DET thereof (the output of voltage detector 302), an output of the op amp U2 becomes low and the FET transistor QF4 is turned off, forcing the first switch 303 to be inactivated. When the inverting input voltage V_{REF} is lower than the non-inverting input voltage DET , the output of the op amp U2 becomes high and the FET transistor QF4 is turned on, turning the first switch circuit 303 on.

[0047] The switch circuit 300 having the switch controller 304' of Fig. 4 performs the same switching operation as that having the switch controller 304 of Fig. 3. Further description of the switch circuit 300 having the controller 304' of Fig. 4 is thus omitted.

Battery Charging Circuit

[0048] Fig. 5 shows an embodiment of a battery charging circuit according to an aspect of the present invention. The battery charging circuit 400 comprises an input terminal 106 to be connected to the AC adaptor 100 and an output terminal 108 to be connected to the battery 200. The battery charging circuit 400 comprises a diode D20, a charging current control unit 410, a current detector 420, a switch 430 and a switch controller 440. The battery charging circuit 400 starts charging the battery 200 with a charging current from the AC adaptor 100.

[0049] The diode D20 is included to prevent a reverse current from the battery 200 to the AC adaptor 100, and has a forward voltage of about 0.5V. For example, the diode D20 may be comprised of either a Schottky diode or a fast recovery diode. The charging current control unit 410 is connected to the input terminal 106 and receives current from the AC adaptor 100 to supply the charging current for the battery 200.

[0050] The current detector 420 detects whether charging current is provided from the charging current control unit 410, and generates a signal IDET as a detection result. The signal IDET is used such that the charging current control unit 410 controls the amount of the charging current in accordance with the voltage level of the signal IDET. The current detector 420 comprises a current detection resistor R17 and an operational amplifier or an "op amp" U3. The current detection resistor R17 is connected in series with the charging current control unit 410, so that it derives from the output current from the unit 410, a voltage value that is proportional to that current.

[0051] One end of the current detection resistor R17 is connected via a resistor R18 to the non-inverting input of the op amp U3. The other end of the current detection resistor R17 is connected via a resistor R20 to the inverting input of the op amp U3. Further, the non-inverting input is connected to ground via a resistor R19, and the output of the op amp U3 is fed back to the inverting input through a resistor R21. With this arrangement, the op amp U3 amplifies the voltage across the current detection resistor R17.

[0052] The switch 430 comprises a P-channel power FET transistor QF5 having an on-state drop voltage of about 0.014V, and a resistor R22. The drain of the FET transistor QF5 is connected via the current detection resistor R17 to the charging current control unit 410 and the source of FET transistor QF5 is connected to the output terminal 108. The gate of the FET transistor QF5 is connected to the switch controller 440. Further, the gate and the source of the transistor QF5 are connected to each other through the resistor R22.

[0053] The source and body of FET transistor QF5 are connected together. Fig. 5 shows the drain - source diode, inherent in a FET transistor, in parallel with the channel.

[0054] Two resistors R23 and R24, one capacitor C1 and an N-channel FET transistor QF6 constitute the switch controller 440. A first end of the resistor R23 is coupled to the output signal IDET from the current detector 420 and the second end of the resistor R23 is connected to the gate of the FET transistor QF6. The FET transistor QF6 has its source grounded and its drain connected to the gate of the FET transistor QF5. The source and body of FET transistor QF6 are connected together. Further, the second end of the resistor R23 is also connected to the ground through the capacitor C1 and the resistor R24 which are connected in parallel to each other.

[0055] The operation of the battery charging circuit 400 will be more fully described below.

[0056] When the AC adaptor 100 and the battery 200 are connected to the computer system, a charge status of the battery 200 is checked, such as by means of an exclusive microcomputer for the battery 200. In the case where the

battery 200 needs to be charged, an operation of charging the battery 200 starts.

Battery Charging

[0057] Once the battery charging operation starts, first, a charging current from the AC adaptor 100 is supplied to the battery 200 through the input terminal 106, the charging current control unit 410, the current detection resistor R17 and the diode D20. At this time, the current detector 420 detects whether the charging current from the charging current control unit 410 is provided. Then, the current detector 420 outputs an output signal IDET of a logic high level as a detection result, so that the FET transistor QF6 of the controller 440 is turned on. This causes a bias voltage to be applied between the gate and the source of FET transistor QF5 which is then turned on. Accordingly, almost all the current from the unit 410 is delivered to the battery 200 through the FET transistor QF5 of through the switch 430 instead of through the diode D20.

[0058] When a current from the AC adaptor 100 is supplied, first, it flows through the diode D20. Then, the current flows through the FET transistor QF5 of the switch 430 instead of through the diode D20. Therefore, power dissipation and loss by the diode D20 can be reduced, and no heat is generated by the diode D20. This will be further described below.

[0059] Referring to Fig. 6, another embodiment of the switch controller of the battery charging circuit is illustrated. The switch controller 440' comprises four resistors R25 to R28, one op amp U4 and an N-channel MOSFET transistor QF7 connected as illustrated in Fig. 6. When an inverting input voltage V_{REF} (such as a voltage used as a power of the microcomputer 501) of the op amp U4 is higher than a non-inverting input voltage IDET thereof, an output of the op amp U4 is at a logic low level and the FET transistor QF7 is turned off, forcing the switch 430 to be turned off. When the inverting input voltage V_{REF} is lower than the non-inverting input voltage IDET, the output of the op amp U4 is at a logic high level and the FET transistor QF7 is turned on, turning the switch 430 on.

[0060] It will be apparent that the battery charging circuit 400 having the switch controller 440' of Fig. 6 performs the same switching operation as that having the switch controller 430 of Fig. 5. The description of the battery charging circuit 400 having the controller 440' of Fig. 6 is therefore omitted.

Effect

[0061] Suppose that a DC voltage of about 19V and a current of about 2.1A are supplied from the AC adaptor 100 and that the output wattage of the adaptor 100 is about 39.9W. As set forth above, the diodes D1 and D20 of the switch circuit 300 and the battery charging circuit 400 have forward voltage drop of about 0.5V each. The FET transistors QF1 and QF5 of the switch and battery charging circuits 300 and 400 may each have an on-state voltage drop of about 0.014V.

[0062] Under these conditions, power dissipation P_{D1} by the diode D1 when conducting 2.1A is about 1.05W (0.5Vx2.1A), and a power loss rate η_{D1} is about 2.63% ((1.05W/39.9W)x100). On the other hand, a power dissipation P_{QF1} by the FET transistor QF1 when conducting 2.1A is about 0.0294W (0.014Vx2.1A), and a power loss rate η_{QF1} is about 0.07% ((0.0294W/39.9W)x100). By using the switch circuit 300 according to the present invention, the power dissipation is reduced by about 1.0206W (1.05W-0.0294W) and the power efficiency is improved by about 2.56% ((1.0206W/39.9W)x100).

[0063] As well known in the art, the battery 200 may be charged in one of two principal modes; specifically, a run and charging mode wherein the battery 200 is charged regardless of the run of the computer system, and a run or charging mode in which the battery 200 is charged depending on the run of the computer system. Suppose that a current of about 1A is supplied from the AC adaptor 100 in the case of the former (the run and charging mode) and that a current of about 2.1A is supplied from the AC adaptor 100 in the case of the latter (the run or charging) mode.

[0064] Under these conditions, the power dissipation P and the power loss rate η by the diode D20 and the FET transistor QF5, when each is respectively conducting the current of 1A or 2.1A as appropriate, in the battery charging circuit 400 will be calculated as follows:

1) in the run and charging mode,

$$P_{D20} = V \times I = 0.5V \times 1A = 0.5W$$

$$\eta_{D20} = (0.5W / 39.9W) \times 100 = 1.25\%$$

$$P_{QF5} = 0.014V \times 1A = 0.014W$$

$$\eta_{QF5} = (0.014W / 39.9W) \times 100 = 0.04\%$$

2) in the run or charging mode,

$$P_{D20} = V \times I = 0.5V \times 2.1A = 1.05W$$

$$\eta_{D20} = (1.05W / 39.9W) \times 100 = 3.63\%$$

$$P_{QF5} = 0.014V \times 2.1A = 0.0294W$$

$$\eta_{QF5} = (0.0294W / 39.9W) \times 100 = 0.07\%$$

[0065] By using the battery charging circuit 400 in the run and charging mode, a power dissipation is reduced by about 0.486W (0.5W-0.014W) and the power efficiency is improved by about 1.22% ((0.486W/39.9W)x100). In the case of the run or charging mode, a power dissipation is reduced by about 1.0206W (1.05W-0.0294W) and the power efficiency is improved by about 2.55% ((1.0206W/39.9W)x100).

[0066] In the case of the run and charging mode, a total power dissipation P_{t1} by the diodes D1 and D20 is about 1.55W (1.05W (P_{D1})+0.5W (P_{D20})) and a total power loss rate η_{t1} by the diodes D1 and D20 is about 3.88% ((1.55W/39.9W) x 100). A total power dissipation P_{t1} by the FET transistor QF1 and QF5 is about 0.0434W (0.0294W(P_{QF1}) +0.014W(P_{QF5})), and a total power loss rate η_{t2} of the FET transistors QF1 and QF5 is about 0.1% ((0.434W/39.9W) x100). Therefore, a total power dissipation is reduced by 1.5W. This enables the wattage of the AC adaptor 100 to be reduced to 38.4W from 39.9W, enabling a smaller, less expensive adaptor to be used, and reducing the amount of power consumed.

[0067] In the case of the run or charging mode, a total power dissipation P_{t3} by the diodes D1 and D20 is about 2.1W (1.05W(P_{D1})+1.05W(P_{D20})) and a total power loss rate η_{t3} of the diodes D1 and D20 is about 5.26% ((2.1W/39.9W) x100).

[0068] A total power dissipation P_{t4} by the FET transistor QF1 and QF5 is about 0.0588W (0.02 94W (P_{QF1}) +0.0294W (P_{QF5})), and a total power loss rate η_{t4} of the FET transistor QF1 and QF5 is about 0.15% ((0.0588W/39.9W)x100). Therefore, a total power dissipation is reduced by 2.04W. This enables the wattage of the AC adaptor 100 to be reduced to 37.86W from 39.9W, enabling a smaller, less expensive adaptor to be used, and reducing the amount of power consumed.

[0069] Furthermore, the heat generated within the computer system is also reduced. Temperature values of each component measured according to the conditions described above, that is, 39.9W, 1A (the run and charging mode) and 2.1A (the run or charging mode), when operating under a room temperature of 26°C are shown in the following tables.

Table 1

	prior art			
	Run&Charging	Run or Charging	Run&Charging	Run or Charging
D1	144°C	144°C	26°C	
D20	85.7°C	144°C	26°C	
QF1			27.7°C	
QF5				34.8°C

Table 2

	prior art			
	Run&Charging	Run or Charging	Run&Charging	Run or Charging
D1	Δ118°C	Δ118°C	0°C	0°C
D20	Δ58°C	Δ118°C	0°C	0°C
QF1			Δ1.7°C	
QF5				Δ8.8°C
Sum	176°C	236°C	1.7°C	8.8°C
(the room temperature is deducted from each device temperature in table 2)				

[0070] As seen in the table 2, the temperature sum is reduced by about 174.3°C (176°C-1.7°C) during the run and charging mode, a temperature sum is reduced by about 227.2°C (236°C-8.8°C) during the run or charging mode.

[0071] Although the present invention has been described with reference to a certain number of particular embodiments, numerous variations and modifications may be made to the circuits of the present invention. For example, the various switches may be implemented as FET transistors (such as MOSFET or JFET transistors), bipolar transistors, mechanical switches such as relays, or other controlled conductivity devices.

[0072] The external power supply may be an AC adaptor connected to a mains AC supply, as described, or any other suitable source of power, such as a generator or a DC supply such as an external 12V battery.

[0073] Furthermore, the invention may be applied to systems having two alternative power sources, either or both of which may be an external power source or a battery. The invention may be applied to systems having more than two alternative power sources, a switching circuit being provided for at least all but one of the power sources, with appropriate control circuitry being provided.

Claims

1. A switch circuit for use with a battery (200) and an external power supply (100), the switch circuit comprising:

   a power supply line (101);

   a diode (D1) coupled in series between the power supply line and a terminal for coupling to an external power supply;

   a switch (303) coupled in parallel with the diode, the switch having a voltage drop when conductive, lower than that of the diode;

   a voltage detector (302) for detecting whether a voltage supplied by an external power supply is higher than a predetermined level, and generating a detection signal (DET) as a result; and

   a switch controller (304) receiving the detection signal, for controlling the ON/OFF condition of the switch so as to bring the switch into an ON condition when the voltage supplied by the external power supply is higher than the predetermined level.

2. A switch circuit for use with a battery (200) and an external power supply (100), the switch circuit comprising:

   a power supply line (101);

   a diode (D1) coupled in series between the power supply line and a terminal for coupling to an external power supply;

   a switch (303) coupled in parallel with the diode, the switch having a voltage drop when conductive, lower than that of the diode;

a current detector (R17) for detecting whether a current supplied by an external power supply is higher than a predetermined level, and generating a detection signal (DET) as a result; and

a switch controller (304) receiving the detection signal, for controlling the ON/OFF condition of the switch so as to bring the switch into an ON condition when the current supplied by the external power supply is higher than the predetermined level.

3. The switch circuit according to claim 1 or claim 2, further comprising:

a second switch (305) for coupling the power supply line to a battery; and

a second switch controller (306) receiving the detection signal, for controlling the ON/OFF condition of the second switch so as to bring the second switch into an OFF condition when the voltage or current supplied by the external power supply is higher than the respective predetermined level.

4. A system, comprising:

a switch circuit according to any of claims 1-3;

a system load;

a battery; and

an external power supply,

wherein power may be supplied to the system load over the power supply line, from either the battery or the external power supply, according to a status of the switching circuit.

5. A system according to claim 4, further comprising a voltage converter coupled to the system load, for controlling a voltage supplied to the system load.

6. A system according to claim 4 or claim 5 being a computer system, wherein the system load comprises a memory, a direct memory access controller and a peripheral.

7. A system according to claim 4, claim 5 or claim 6, being a portable system.

8. A battery charging circuit comprising:

a first terminal (106) for coupling to an external power supply;

a second terminal (108) for coupling to a battery (200); and

a switch circuit according to claim 1, or claim 2, or claim 3, wherein the diode and the power supply line are coupled in series between the first terminal and the second terminal.

9. A method of operating a switch circuit for providing power from a power supply (100) to a power supply line (104), the switch circuit comprising

- a diode (D1) coupled in series between the power supply line and a terminal (101) for coupling to the power supply; and
- a switch (303) coupled in parallel with the diode, the switch having a voltage drop when conductive, lower than that of the diode;

the method comprising the steps of:

- detecting whether a voltage, or a current, supplied by the power supply is higher than a predetermined level; and

- controlling the ON/OFF condition of the switch so as to bring the switch into an ON condition when the voltage, or current, respectively, supplied by the external power supply is higher than the predetermined level.

10. A switch circuit or a system or a battery charger or a method as described and/or as illustrated in Figs 3-6 of the accompanying drawings.

Fig. 1

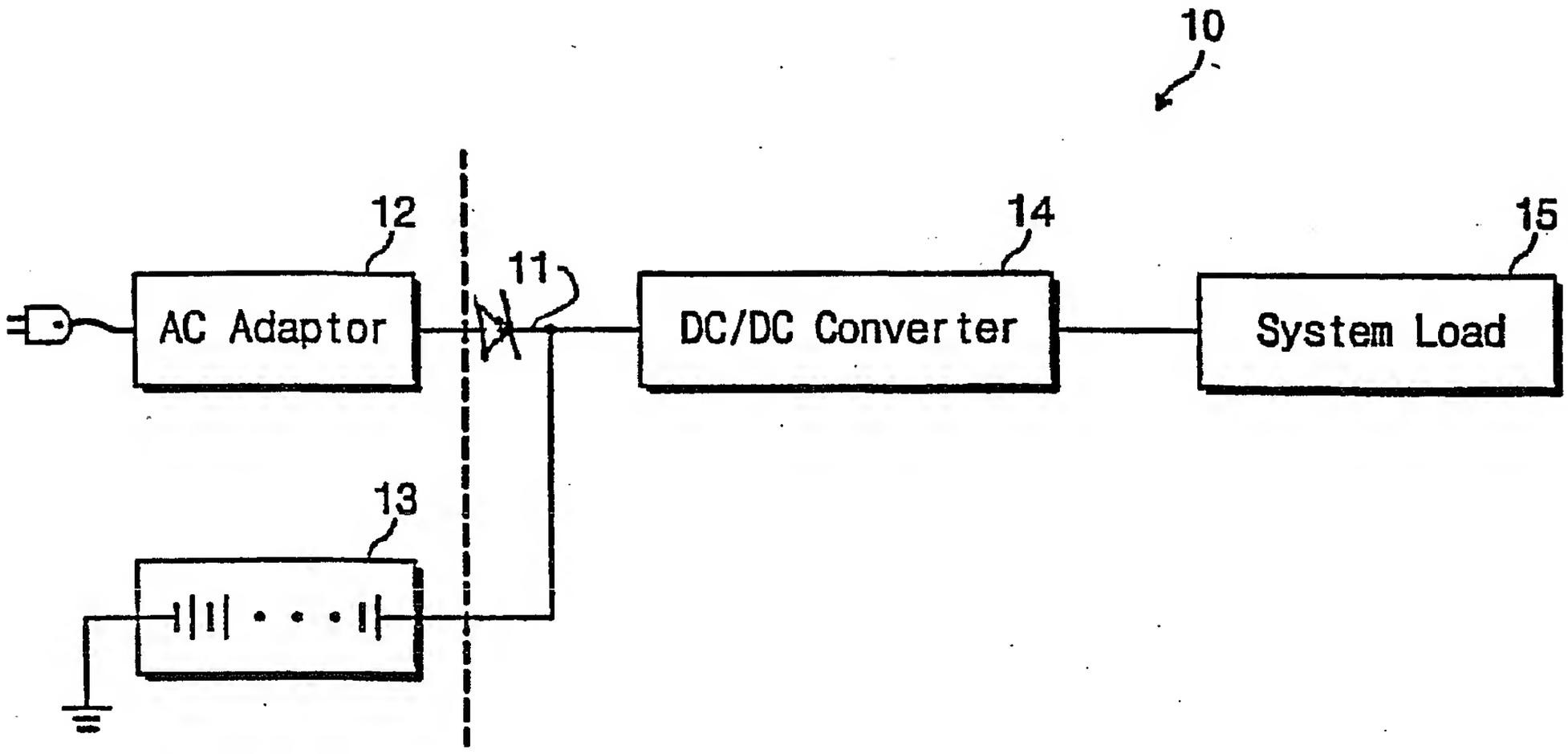

Fig. 2

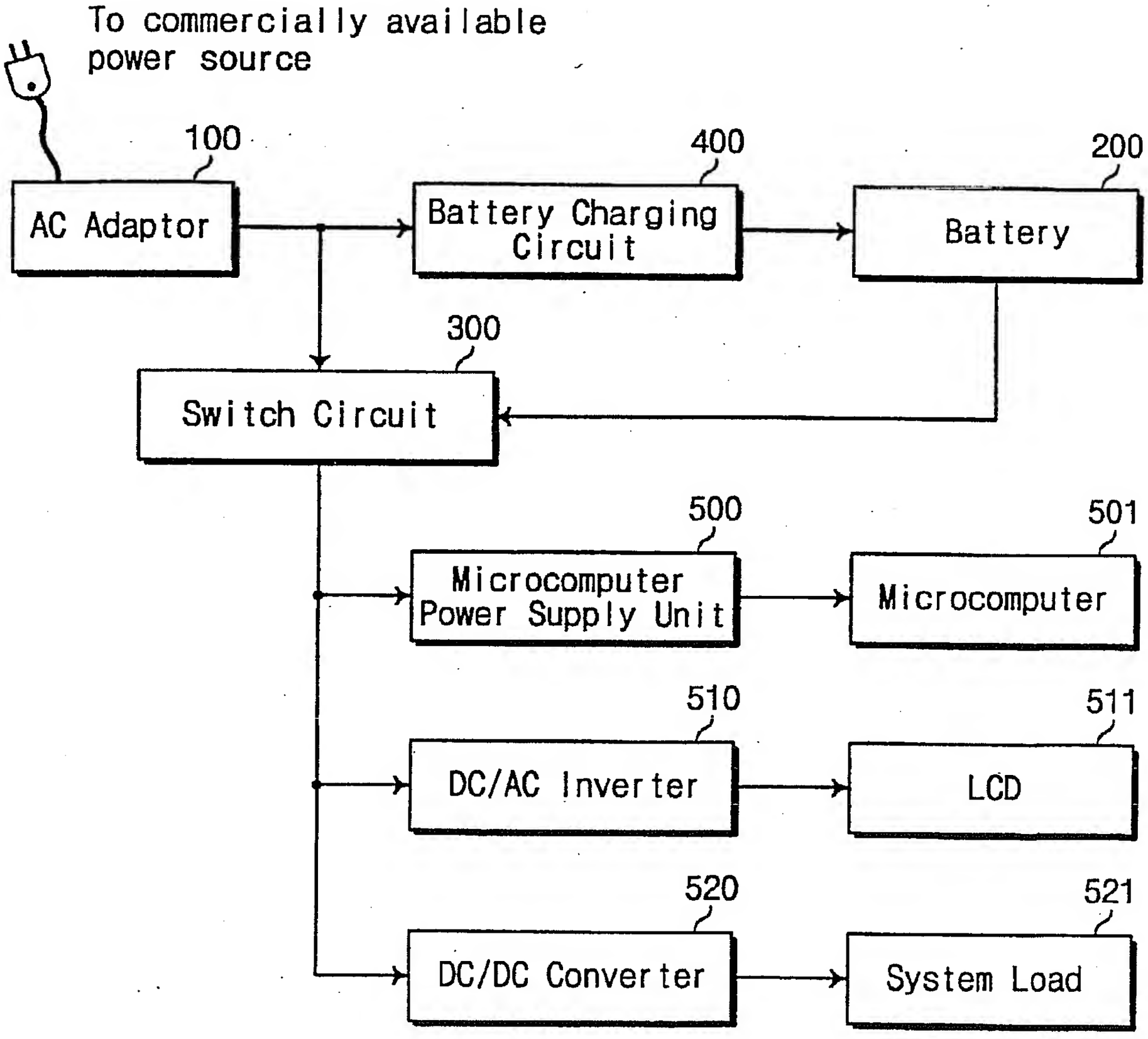
To commercially available
power source
100
AC Adaptor
400
Battery Charging Circuit
200
Battery
300
Switch Circuit
500
Microcomputer Power Supply Unit
501
Microcomputer
510
DC/AC Inverter
511
LCD
520
DC/DC Converter
521
System Load

Fig. 3

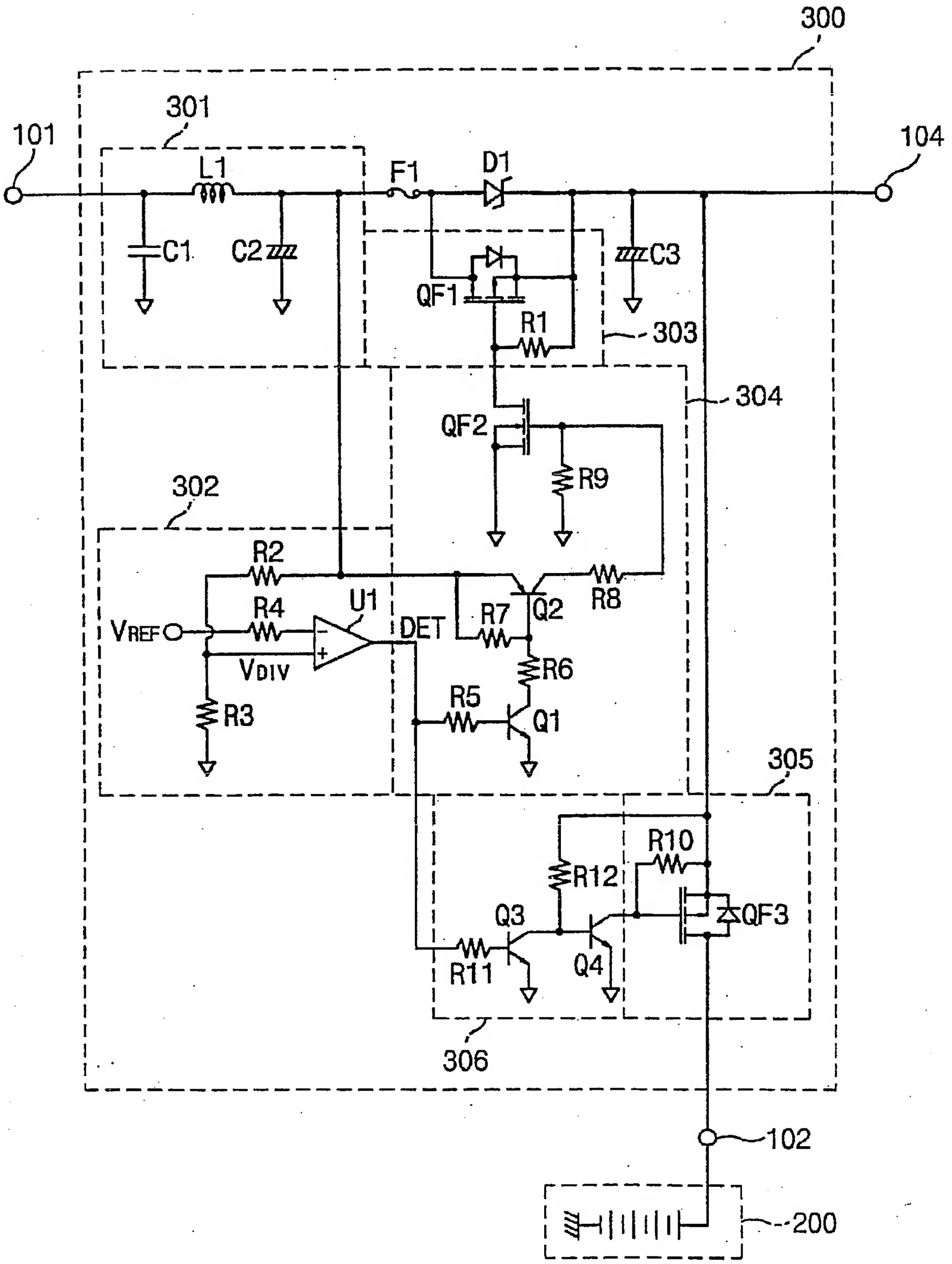
300
301
101
104
L1
F1
D1
C1
C2
C3
QF1
R1
303
304
QF2
R9
302
R2
R4
U1
R8
R7
Q2
VREF
DET
VDIV
R6
R5
Q1
R3
305
R10
R12
QF3
Q3
Q4
R11
306
102
200

Fig. 4

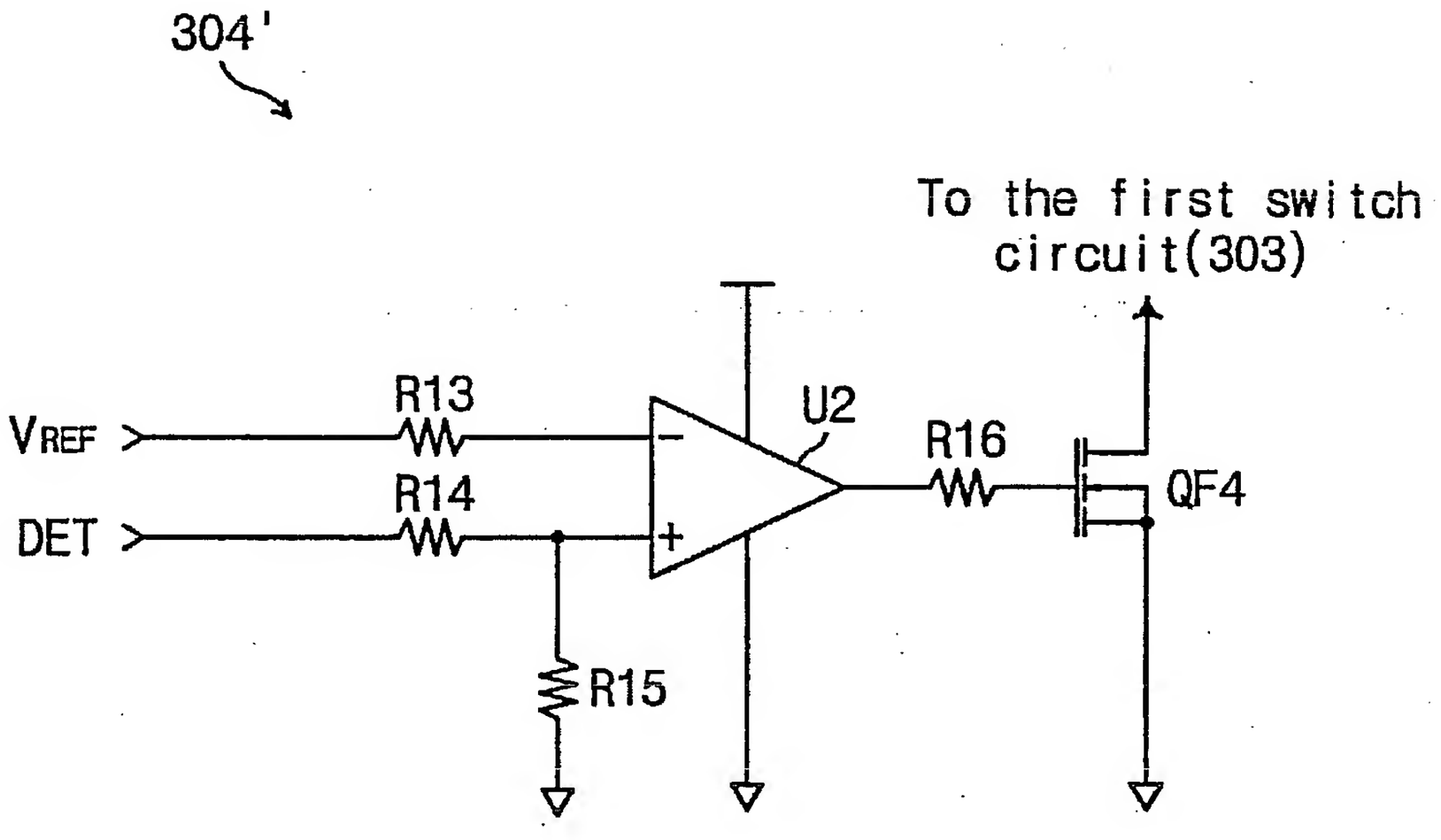
304'
To the first switch circuit(303)
VREF
DET
R13
R14
R15
U2
R16
QF4
-
+

Fig. 5

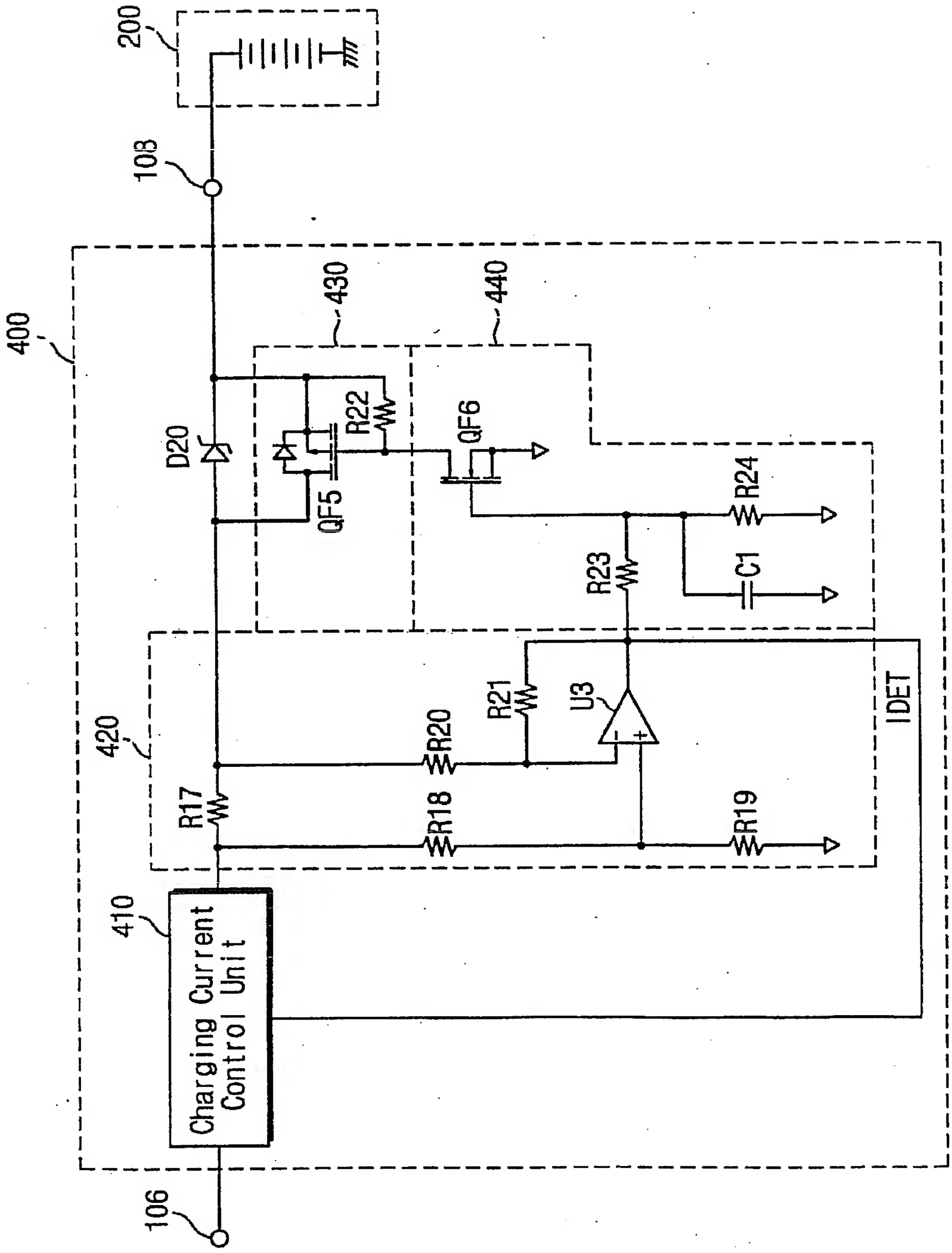
200
103
400
430
440
D20
R22
QF6
QF5
R24
R23
C1
420
R21
U3
R20
IDET
R17
R18
R19
410
Charging Current Control Unit
106

Fig. 6